CASAMBI

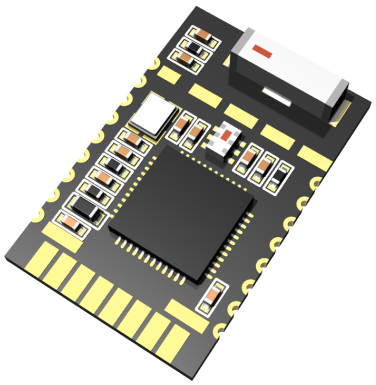
Casambi CBM-001

Product Specification

Features

Casambi Lighting Control System:

- Wirelessly controllable with a Bluetooth 4.0 smart device
- No need for external gateway device
- Forms automatically a wireless mesh network
- Device firmware can be updated over-the-air
- Casambi cloud service available
- Extremely easy set-up



CBM-001 Features:

- Small form factor, 12,7 mm x 20,0 mm x 2,85 mm
- 12 pcs general purpose input/output pins
- SPI, TWI, UART, PWM (max. 4 ch), ADC (max. 3 ch)
- Integrated antenna with optional matching circuitry
- Up to 4 dBm output power and RX sensitivity -93 dBm
- Range up to 60 m in open air
- Can be mounted in horizontal or vertical position
- Delivered pre-loaded with Casambi firmware

Applications

- LED drivers, 1-4 channels
- Different lighting control applications
- Light fixtures
- Single and multicolor LED bulbs

1 Description

CBM-001 is a Class 2 embedded Bluetooth 4.0 module designed to be integrated into LED drivers, different lighting control applications, light fixtures and LED bulbs. It is pre-programmed with Casambi's proprietary firmware making it completely compatible with other Casambi enable devices.

CBM-001 is controlled wirelessly with Casambi smartphone and tablet applications using Bluetooth 4.0 protocol. Devices form automatically a self-healing and self-organizing wireless mesh network so that a large number of fixtures can be controlled from any point. No external gateway module is needed.

CBM-001 contains a powerful 32 bit ARM® Cortex™-M0 CPU and a 2.4 GHz transceiver with on-board antenna and optional matching circuitry. Different external components, such as motion detectors, ambient light sensors and PWM circuits, can be interfaced with the module by using its 12 general purpose I/O pins.

CBM-001 can be mounted both in horizontal and vertical position making it very versatile for projects with different form-factors.

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2 Revision history

Date	Version	Description
January 2014	0.1	Preliminary Product Specification
December 2014	1.0	Original Version
May 2015	1.1	Current consumption and operating temperature updated
June 2015	1.2	Number of PWM channels updated to up to four
September 2015	1.3	Changes to pages 1, 5, 8, 10, 16 and 19
June 2016	1.4	Added chapter 16.1. Changes to chapters 16.2. and 16.3
December 2016	1.5	Modified POR resistor value in chapter 16.1

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3 Operation

Casambi CBM-001 is an embedded wireless module with a powerful 32 bit ARM® Cortex™-M0 CPU and a 2.4 GHz transceiver with on-board antenna and optional matching circuitry. It can be integrated, for example, into a LED driver, light fixture or LED bulb.

CBM-001 has total of 12 GPIO pins, which can be configured to perform various tasks, such as SPI, TWI (I^2C compatible), UART, 4 channel PWM output and 3 channel Analog-to-Digital Converter input. Only the ADC input channels have fixed GPIO pins. Other functions can be freely configured to any GPIO pin.

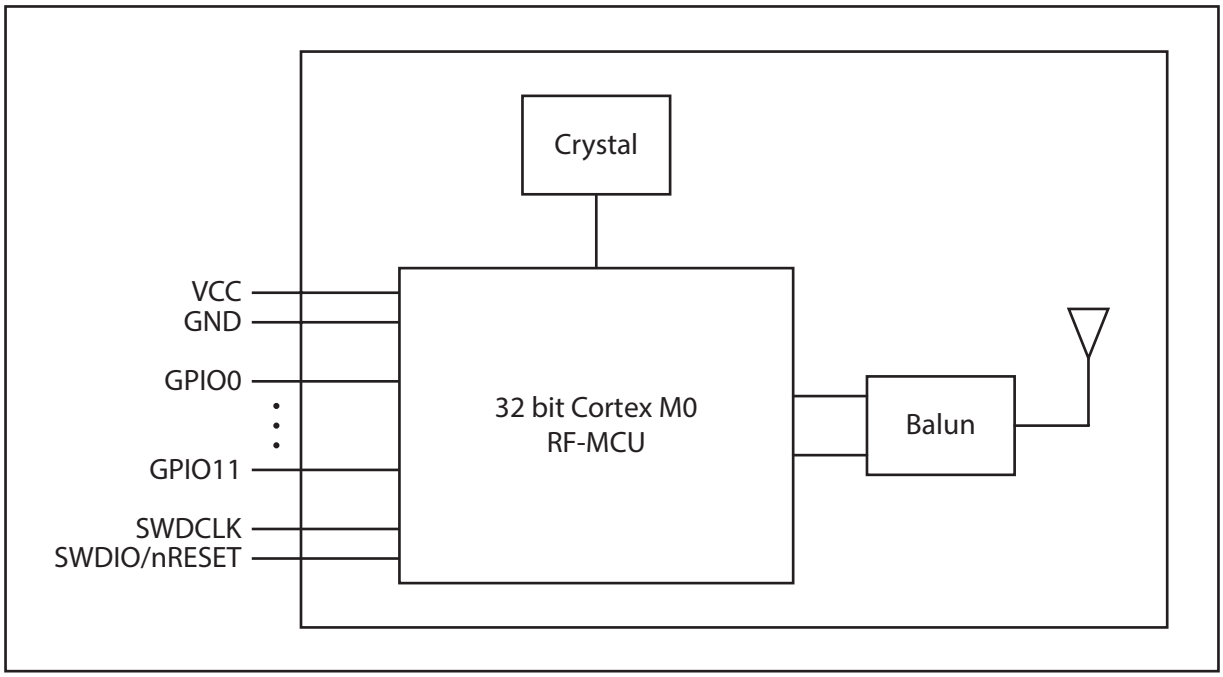
CBM-001 is controlled wirelessly by a smart device with Casambi application. Multiple Casambi units form automatically a mesh network, which can be controlled from any point. The network communicates directly with the smart device using Bluetooth 4.0. No external gateway device or Wireless LAN network is needed.

CBM-001 has an integrated 2,4 GHz antenna. This will have to be taken into account when the device is integrated to any environment. See chapter "16.2 Mounting" for further instructions.

The module can be operated also from a traditional on/off wall switch. By flicking the switch on and off the user can select different pre-set modes. These modes can affect one or several devices on the network. This way the user does not have to have the smart device at hand all the time in order to select the desired settings or modes. This feature requires an external electrolytic capacitor to supply power during power-off stage as well as a power-on detection circuitry.

A large number of different setting of CBM-001 can be configured in Casambi Admin webpages and taken into use without a need to re-program the module. These settings include, but are not limited to, I/O pin mapping, ADC, PWM, push button, etc.

4 Block Diagram



Picture 1. CBM-001 block diagram

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5 System Blocks

5.1 General Purpose I/O (GPIO)

CBM-001 has 12 General Purpose I/O pins. Each GPIO can be accessed individually and each has the following features:

- Input/output direction
- Output drive strength
- Internal pull-up and pull-down resistors
- Trigger interrupt on all pins (rising edge, falling edge, any change)
- Serial interface and PWM output can be freely configured to each pin

GPIO pins 0-2 also supports analog input signals when an internal Analog-to-Digital Converter (ADC) is used. If external voltage reference preferred, it can be connected to GPIO 3.

5.2 Analog-to-Digital Converter (ADC)

The 10 bit incremental Analog-to-Digital Converter enables sampling of up to 3 external signals (GPIOs 0-2) through a front end multiplexer. The ADC has configurable input and reference prescaling, and sample resolution (8, 9, and 10 bit).

There are three options for the voltage reference:

- Internal 1,20 V reference
- External 1,20 V reference
- VCC with 1/3 prescaling

Analog inputs can have 1/3 prescaling, 2/3 prescaling or no prescaling.

5.3 Temperature Sensor

The temperature sensor measures silicon die temperature over the temperature range of the device with 0,25°C resolution.

5.4 PWM Output

Any GPIO pin can be configured to output PWM signal. Up to 4 PWM channels can be used simultaneously. PWM frequency can be determined freely up to 40 kHz. By default the PWM frequency is the same with all PWM channels. The maximum resolution is 400-1600 steps and it depends on the PWM frequency.

The PWM signal is logic level (max. V_{CC}) and it has driving capacity from 0,5 mA (standard) up to 15 mA (high-drive).

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6 Serial Interfaces

CBM-001 offers multiple serial interfaces for connecting external peripherals, such as sensors and memory ICs. The module supports 3-wire Serial Peripheral Interface (SPI), Two-Wire Interface (TWI) and UART.

Maximum of two SPI or TWI interface buses can be used in one application. They can both be SPI or TWI, or there can be one of each. UART works separately from the SPI and TWI interfaces.

6.1 Serial Peripheral Interface (SPI)

CBM-001 supports a 3-wire (SCK, MISO, MOSI) bidirectional SPI bus with fast data transfers to and from multiple slaves. CBM-001 acts as a master and it provides a simple CPU interface which includes a TXD register for sending data and an RXD register for receiving data. These registers are double buffered to enable some degree of uninterrupted data flow in and out of the SPI master.

Each of the slave devices requires an individual chip select signal which can be connected to any available GPIO pin. The SPI master does not implement support for chip select directly. Therefore the correct slave must be selected independently of the SPI master.

The GPIOs used for each SPI interface line can be chosen from any GPIO on the module and are independently configurable. This enables great flexibility in module pinout and enables efficient use of printed circuit board space and signal routing.

The SPI peripheral supports SPI modes 0, 1, 2, and 3.

6.2 Two-Wire Interface (TWI)

The Two-Wire Interface (I^2C compatible) can interface a bidirectional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 128 individually addressable devices. The interface is capable of clock stretching and data rates of 100 kbps and 400 kbps are supported.

The GPIOs used for each Two-Wire Interface line can be chosen from any GPIO on the module and are independently configurable. This enables great flexibility in module pin-out and enables efficient use of board space and signal routing.

6.3 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in HW up to 1 Mbps baud. Parity checking and generation for the 9th data bit are supported.

The GPIOs used for each UART interface line can be chosen from any GPIO on the module and are independently configurable. This enables great flexibility in module pinout and enables efficient use of board space and signal routing.

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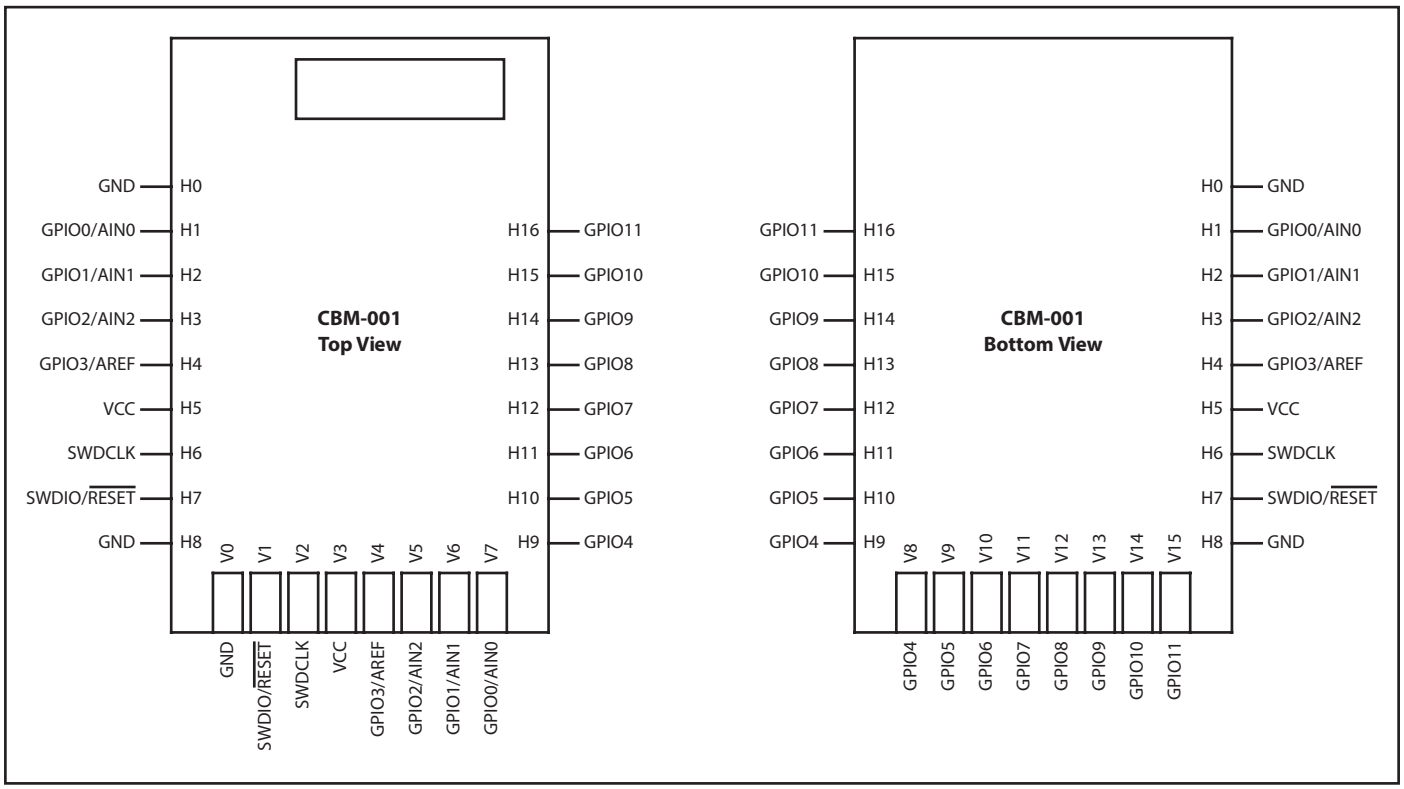
7 Pin Assignment



Picture 2. Pin assignment

Horizontal Pin	Vertical Pin	Pin Name	Pin Function	Description
H0	-	GND	Power	Ground
H1	V7	GPIO0 AIN0	Digital I/O Analog input	General purpose I/O pin ADC input 0
H2	V6	GPIO1 AIN1	Digital I/O Analog input	General purpose I/O pin ADC input 1
H3	V5	GPIO2 AIN2	Digital I/O Analog input	General purpose I/O pin ADC input 2
H4	V4	GPIO3 AREF	Digital I/O Analog input	General purpose I/O pin ADC external reference voltage
H5	V3	VCC	Power	Power supply
H6	V2	SWDCLK	Digital input	HW debug and flash programming I/O
H7	V1	SWDIO nRESET	Digital I/O Analog input	HW debug and flash programming I/O System reset (active low)
H8	V0	GND	Power	Ground
H9	V8	GPIO4	Digital I/O	General purpose I/O pin
H10	V9	GPIO5	Digital I/O	General purpose I/O pin
H11	V10	GPIO6	Digital I/O	General purpose I/O pin

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Horizontal Pin	Vertical Pin	Pin Name	Pin Function	Description
H12	V11	GPIO7	Digital I/O	General purpose I/O pin
H13	V12	GPIO8	Digital I/O	General purpose I/O pin
H14	V13	GPIO9	Digital I/O	General purpose I/O pin
H15	V14	GPIO10	Digital I/O	General purpose I/O pin
H16	V15	GPIO11	Digital I/O	General purpose I/O pin

Table 1. Pin assignment

8 Electrical Specifications

8.1 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which CBM-001 can be exposed without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the CBM-001.

Absolute Maximum Ratings	Min.	Max.	Units
Supply voltage, V_{CC}	-0,3	+3,9	V
GND		0	V
I/O pin voltage, V_{IO}	-0,3	V_{CC} + 0,3	V
Storage temperature	-40	+125	°C
Operating temperature, T_A	-25	+75	°C

Table 2. Absolute maximum ratings

8.2 Power Supply Specifications

Power Supply Specifications	Min.	Typ.	Max.	Units
Supply voltage, V_{CC}	+2,5	+3,0	+3,6	V
Supply current, I_{CC}				
Active state, CPU + RX/TX (Casambi active)		15	20,4	mA
Idle, only CPU running		1,5	2,0	mA

Table 3. Power supply specifications

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8.3 General Purpose I/O Specifications

GPIO Specifications	Min.	Typ.	Max.	Units
Input high voltage, V_{IH}	0,7 V_{CC}		V_{CC}	V
Input low voltage, V_{IL}	GND		0,3 V_{CC}	V
Output high voltage, V_{OH}	V_{CC}-0,3		V_{CC}	V
Output low voltage, V_{OL}	GND		0,3	V
Source current, I_{GPIO_OUT}		0,5	5 [1)]	mA
Sink current, I_{GPIO_IN}		0,5	5 [1)]	mA
Pull-up resistance, R_{PU}	11	13	16	kΩ
Pull-down resistance, R_{PD}	11	13	16	kΩ

Table 4. GPIO specifications

1) Total source/sink current of all GPIO pins combined is 15 mA. If required source/sink current in any GPIO pin is more than 0,5 mA, corresponding GPIO pin must be configured as high-drive.

9 Environmental Conditions

Environmental Conditions	Min.	Typ.	Max.	Units
Storage temperature	-40		+125	°C
Operating temperature, T_A	-25	+25	+85	°C
Relative humidity, storage			90	%
Relative humidity, operating			90	%

Table 5. Environmental conditions

10 Radio Characteristics

10.1 General Radio Characteristics

General Radio Characteristics	Min.	Typ.	Max.	Units
Operating frequencies, f_{OP}, 1 MHz chann. spacing	2400		2483	MHz
PLL programming resolution, PLL_{res}		1		MHz
Frequency deviation, Δf_{BLE}	±225	±250	±275	kHz
On-air data rate, bps_{FSK}	250		2000	kbps

Table 6. General radio characteristics

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10.2 Radio Current Consumption

Radio Current Consumption	Min.	Typ.	Max.	Units
TX only run current @ POUT = +4 dBm [1)]		16		mA
TX only run current @ POUT = 0 dBm [1)]		10,5		mA
TX only run current @ POUT = -4 dBm		8		mA
TX only run current @ POUT = -8 dBm		7		mA
TX only run current @ POUT = -12 dBm		6,5		mA
TX startup current		7		mA
RX only run current		13		mA
RX startup current		8,7		mA

Table 7. Radio current consumption

10.3 Transmitter Specifications

Transmitter Specifications	Min.	Typ.	Max.	Units
Maximum output power, P_{RF}		4		dBm
RF power control range, P_{RFC}	20	24		dB
RF power accuracy, P_{RFCR}			±4	dB

Table 8. Transmitter specifications

11 Communication Interface Characteristics

11.1 UART Specifications

UART Specifications	Min.	Typ.	Max.	Units
Run current @ max baud rate, I_{UART1M}		230		µA
Run current @ 115200 bps, $I_{UART115k}$		220		µA
Run current @ 1200 bps, $I_{UART1k2}$		210		µA
Baud rate for UART, f_{UART}	1,2		921,6	kbps

Table 9. UART specifications

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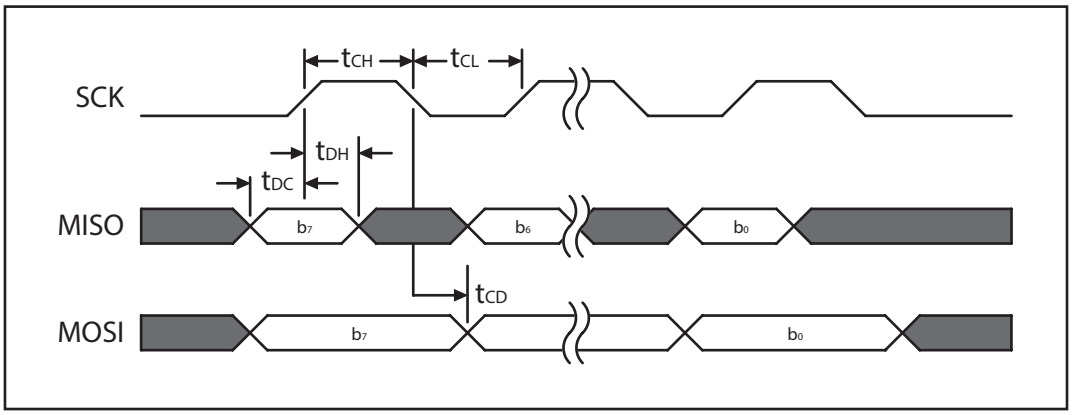
11.2 SPI Specifications

SPI Specifications	Min.	Typ.	Max.	Units
Run current for SPI master @ 125 kbps, $I_{SPI125K}$		180		µA
Run current for SPI master @ 8 Mbps, I_{SPI8M}		200		µA
Bit rates for SPI, f_{SPI}	0,125		8	Mbps

Table 10. SPI specifications



Picture 3. SPI timing diagram, one byte transmission, SPI mode 0

SPI Timing Parameters	Min.	Typ.	Max.	Units
Data to SCK setup, t_{DC}	10			ns
SCK to Data hold, t_{DH}	10			ns
SCK to Data valid, t_{CD}	60		80	ns
SCK High time, t_{CH}	40			ns
SCK Low time, t_{CL}	40			ns
SCK Frequency, f_{SCK}	0,125		8	MHz
SCK Rise and Fall time, t_R, t_F			100	ns

Table 11. SPI timing parameters

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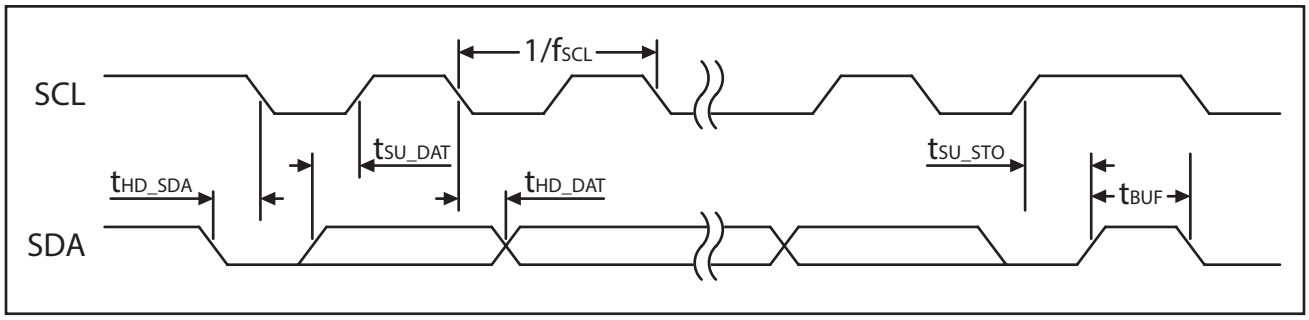
11.3 TWI Specifications

TWI Specifications	Min.	Typ.	Max.	Units
Run current for TWI @ 100 kbps, I_{2W100K}		380		µA
Run current for TWI @ 400 kbps, I_{2W400K}		400		µA
Bit rates for TWI, f_{2W}	100		400	kbps

Table 12. TWI specifications



Picture 4. TWI SCL/SDA timing

TWI Timing Parameters	Standard Min.	Standard Max.	Fast Min.	Fast Max.	Units
SCL clock frequency, f_{SCL}		100		400	kHz
Hold time for START and repeated START condition, t_{HD_STA}	5200		1300		ns
Data setup time before positive edge on SCL, t_{SU_DAT}	300		300		ns
Data hold time after negative edge on SCL, t_{HD_DAT}	300		300		ns
Setup time from SCL goes high to STOP condition, t_{SU_STO}	5200		1300		ns
Bus free time between STOP and START conditions, t_{BUF}	4700		1300		ns

Table 13. TWI timing parameters

12 Temperature Sensor Specifications

Temperature Sensor Specifications	Min.	Typ.	Max.	Units
Run current for Temperature sensor, I_{TEMP}		185		µA
Time required for temp. measurement, t_{TEMP}		35		µs
Temperature sensor range, T_{RANGE}	-25		+75	°C
Temperature sensor accuracy, T_{ACC}	-4		+4	°C
Temperature sensor resolution, T_{RES}		0,25		°C

Table 14. Temperature sensor specifications

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13 Analog-to-Digital Converter (ADC) Specifications

ADC Specifications	Min.	Typ.	Max.	Units
Differential non-linearity (10 bit mode), DNL_{10b}		<1		LSB
Integral non-linearity (10 bit mode), INL_{10b}		2		LSB
Offset error, V_{OS}	-2		+2	%
Gain error, e_G	-2		+2	%
Internal reference voltage, V_{REF_INT}	-1,5	1,20 V	+1,5	%
Internal reference voltage drift, TC_{REF_INT}	-200		+200	ppm/°C
External reference voltage, V_{REF_EXT}	0,83	1,20	1,30	V
Time required to convert a single sample in 10 bit mode, t_{ADC10b}		68		µS
Time required to convert a single sample in 9 bit mode, t_{ADC9b}		36		µS
Time required to convert a single sample in 8 bit mode, t_{ADC9b}		20		µS
Current drawn by ADC during conversion, I_{ADC}		290		µA

Table 15. ADC specifications

14 PWM Specifications

PWM Specifications	Min.	Typ.	Max.	Units
PWM frequency, f_{PWM}			40	kHz
PWM high output voltage, V_{PWM_H}	V_{CC}-0,3		V_{CC}	V
PWM low output voltage, V_{PWM_L}	GND		0,3	V
PWM sink/source current, I_{PWM}		0,5	15 [1)]	mA
PWM resolution	400		1600	steps
PWM resolution @ f_{PWM} 10 kHz			1600	steps
PWM resolution @ f_{PWM} 20 kHz			800	steps
PWM resolution @ f_{PWM} 40 kHz			400	steps

Table 16. PWM specifications

[1)] Total source/sink current of all GPIO pins combined is 15 mA. If required source/sink current in any GPIO pin is more than 0,5 mA, corresponding GPIO pin must be configured as high-drive.

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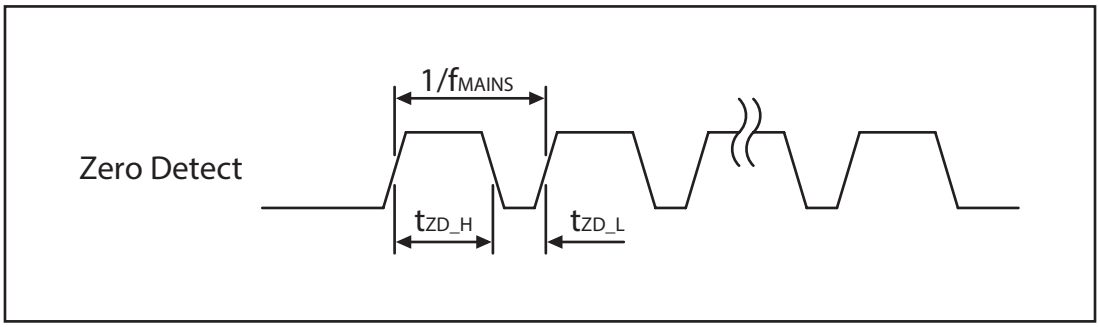
15 Zero Detect Characteristics

Zero Detect Characteristics	Min.	Typ.	Max.	Units
Zero Detect high voltage, V_{ZD_H}	V_{CC}-0,3		V_{CC}	V
Zero Detect low voltage, V_{ZD_L}	GND		0,3	V
Zero Detect frequency, f_{MAINS}		50		Hz
Zero Detect High time, t_{ZD_H}	1		20	ms
Zero Detect Low time, t_{ZD_L}	1		20	ms

Table 17. Zero Detect characteristics



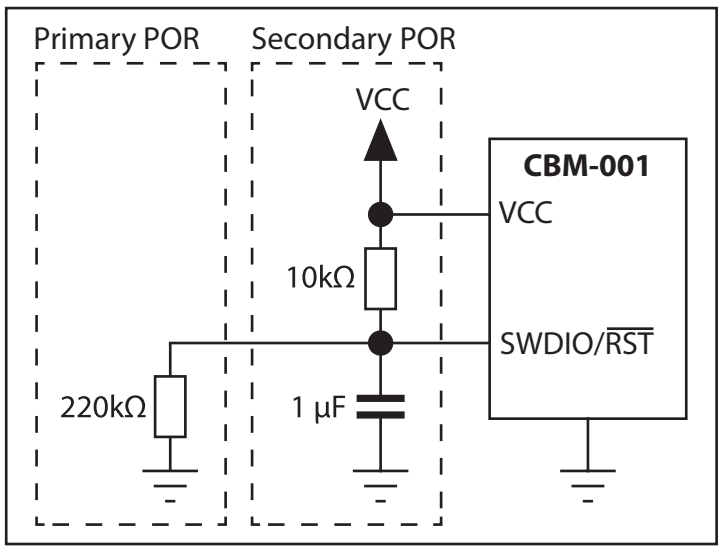
Picture 5. Zero Detect timing

16 Application Information

16.1 Power-On Reset (POR)

Sometimes different external factors may cause unwanted resets to the system. To avoid this, an external Power-on reset (POR) circuitry should be added. At simplest, the POR can be achieved by adding a single 220kΩ resistor between SWDIO/nRST pin and ground.

In addition, it is a good practise to add place-holders for a secondary POR circuit components. This circuit acts as a back-up POR circuit if the single resistor is not adequate. The secondary POR circuit consist of a pull-up resistor (10kΩ) from SWDIO/nRST to VCC and a bypass capacitor (1 µF) from SWDIO/nRST to GND.



Picture 6. Power-on reset circuitry

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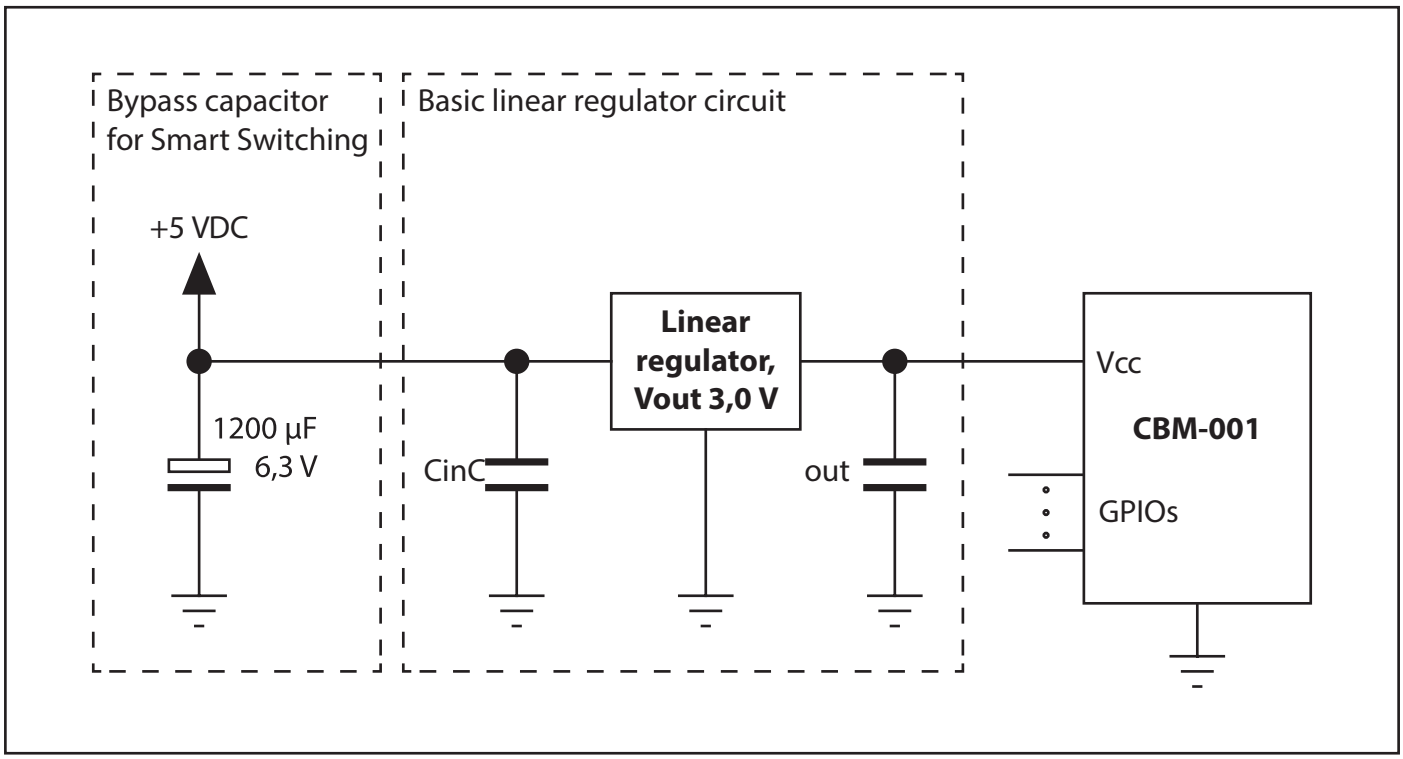
16.2 Smart Switching

Casambi has developed a solution for controlling lighting with only a traditional on/off wall switch. By default the wall switch can be used to dim the lights, but different settings can be selected from Casambi App, such as selecting a pre-set mode. With Smart Switching feature multiple lights can be controlled from a single switch. Smart Switching feature is used by flicking the wall switch quickly off and on.

Smart Switching is a function which requires an external electrolytic bypass capacitor and a power-on detection circuitry in order to work. The external electrolytic capacitor is needed to supply the necessary operating voltage for the module during power-off stage. It can be either an external capacitor just for the CBM-001, or it can be a part of a larger power supply on the host board. If the capacitor is dedicated just for the CBM-001, the minimum required capacitance is 1200 µF. It is advisable to connect the capacitor before any voltage regulation for larger voltage drop.

Even if Smart Switching feature is not used, the correct use of CBM-001 still requires the power-on detection and the external capacitor. These are needed so that the module can inform Casambi network when its power is cut off. The external capacitor will provide power to the module a short time after the power has been switched off. A suitable time for Smart Switching is 1,5 seconds and without Smart Switching 0,5 seconds. The external capacitor will have to be sized according to these requirements.

It is a good practice to use a capacitor with temperature range up to 105°C.



Picture 7. Powering CBM-001 with an external capacitor for Smart Switching

16.3 Power-On Detection

In order to operate correctly, the Casambi network will have to know if power has been switched off from some unit. For this reason the unit will have to know when its power has been switched off. This is done by power-on detection together with an external capacitor (see previous chapter).

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In case of CBM-001 the power-on detection is a signal that is connected to any GPIO pin. The signal can be one of the following four types:

- constant high signal when power is present, low signal when power is absent
- constant low signal when power is present, high signal when power is absent
- pulsed 100 Hz square wave signal when power is present, constant low signal when power is absent
- pulsed 100 Hz square wave signal when power is present, constant high signal when power is absent

The power-on signal can be derived from either DC or AC mains voltage. If the host application is mains powered, so called Zero Detect circuitry shall be designed. The Zero Detect circuitry is connected to mains voltage and it detects when the voltage crosses the zero point. This information is needed to determine when the wall switch has been switched off and when it is switched back on. CBM-001 requires two Zero Detect pulses on each mains cycle, so the mains voltage will have to be full-wave rectified. Also the use of a schmitt trigger is strongly advised in order to get clean pulses.

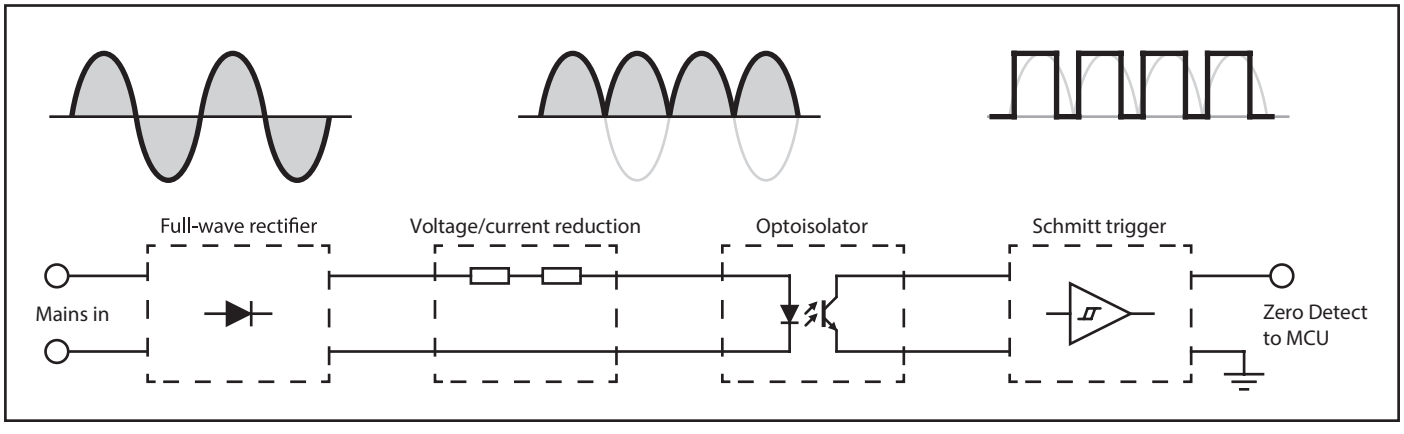
Only a block diagram of the Zero Detect circuitry is provided on this datasheet. This is because the application and the surrounding electronics may vary greatly which makes it impossible to provide a solution that works on every application. The block diagram shows the basic concept of an isolated Zero Detect circuitry. The mains voltage is first full-wave rectified, then dropped to the suitable level for the optoisolation. After the isolation the signal is filtered with a schmitt trigger.

The designer of the host system will have to design a suitable Zero Detect circuitry. If the host system is isolated, the Zero Detect signal will have to be isolated as well. Extreme caution will have to be used when working with Zero Detect since potentially lethal mains voltages are involved.

The voltage level of the Zero Detect signal will have to be suitable for CBM-001, and it will have to have two pulses on each mains cycle. CBM-001 detect only the rising edge of the Zero Detect pulses, so the pulse width can be chosen freely as long as it goes low for at least 1 ms. Zero Detect signal can be connected to any free GPIO pin on CBM-001.

Use of the external capacitor and Zero Detect circuitry is strongly advised. In addition to Smart Wall Switch feature they enable faster response to the power-off condition. When the mains voltage is cut out from the device with CBM-001, the capacitor supplies enough power for the module to send status update to the network. This way the status of the module is immediately updated to offline on the Casambi application.

If the external capacitor and Zero Detect circuitry is omitted, the module will have to send status information to the network periodically which causes a delay to the status update on the application as well as unnecessary traffic on the network.



Picture 8. Block diagram of an isolated Zero Detect circuitry.

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16.4 Mounting

CBM-001 has two sets of soldering pads, which allows it to be mounted both in horizontal and vertical position. In some application, such as LED drivers, there are large components which could affect the antenna performance greatly if the module is mounted at the bottom of the device horizontally on the main PCB. Also horizontally mounted module has much larger footprint compared to vertically mounted module.

For such cases the module can be mounted in vertical position, either by using a 1,27 mm pitch pin header, or by soldering the module directly into a routed slot on the main PCB.

When mounted in horizontal position there will have to be two keep-out areas; one for the antenna and one for the unused pads used for vertical assembly.

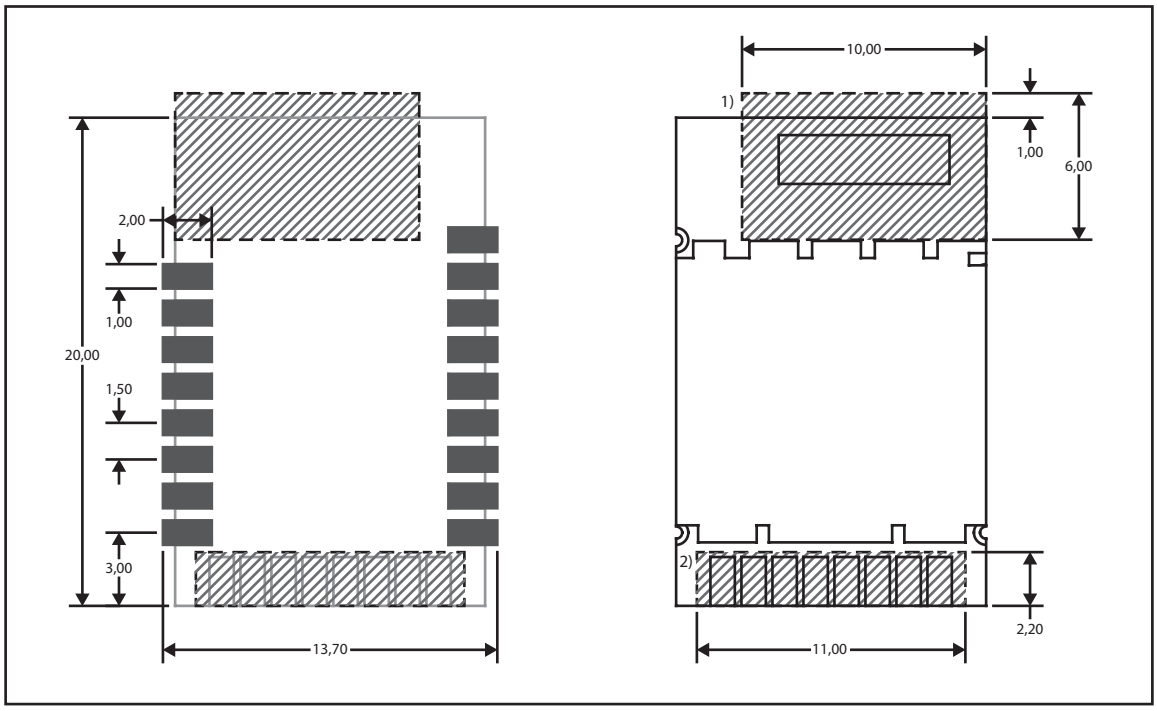
16.4.1 Horizontal Mounting

When CBM-001 is mounted in a horizontal position it is soldered in by using the soldering pads on both long sides of the module. The soldering pads are designed so that the module can be both hand and reflow soldered.

When mounted in a horizontal position, there are two mandatory keep-out areas involved. One is for antenna and the other is for bottom side soldering pads at the narrow end of the module. These pads are used for vertical assembly.

The antenna keep-out applies to all layers of the mother board. There shall not be any components, traces, pads or copper areas in any layer within the keep-out area.

The keep-out area for the soldering pads applies only to the outer surface of the mother board.



Picture 9. Recommended land pattern for horizontal assembly and required keep-out areas

1) This keep-out area will have to be kept clear from any parts, traces and copper on all layers.
2) This keep-out area applies only to the layer closest to the module.

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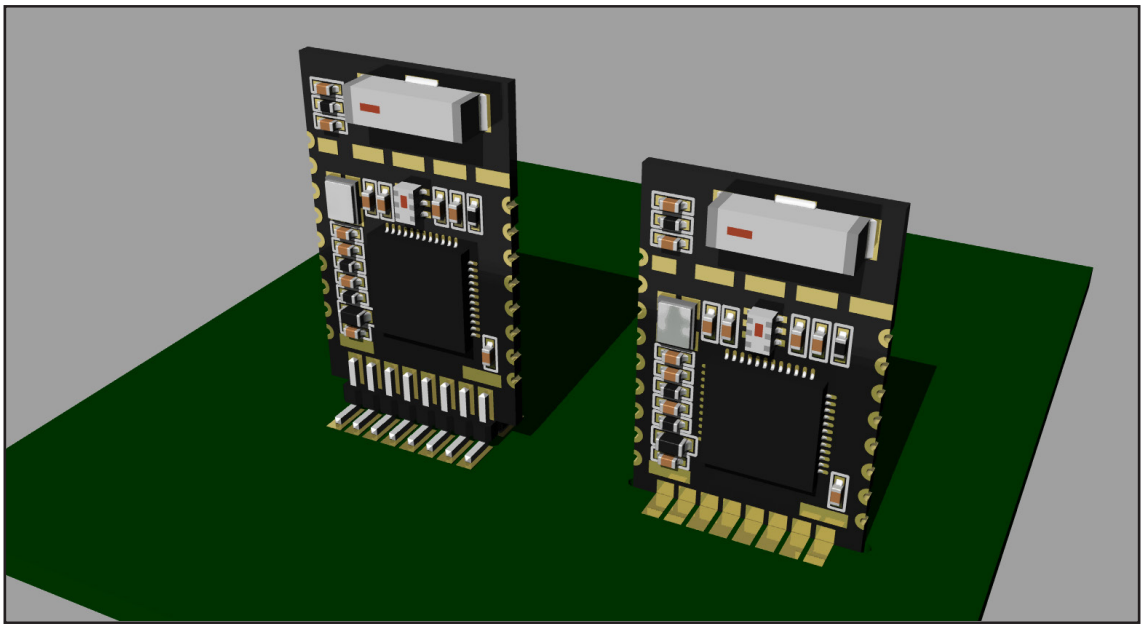
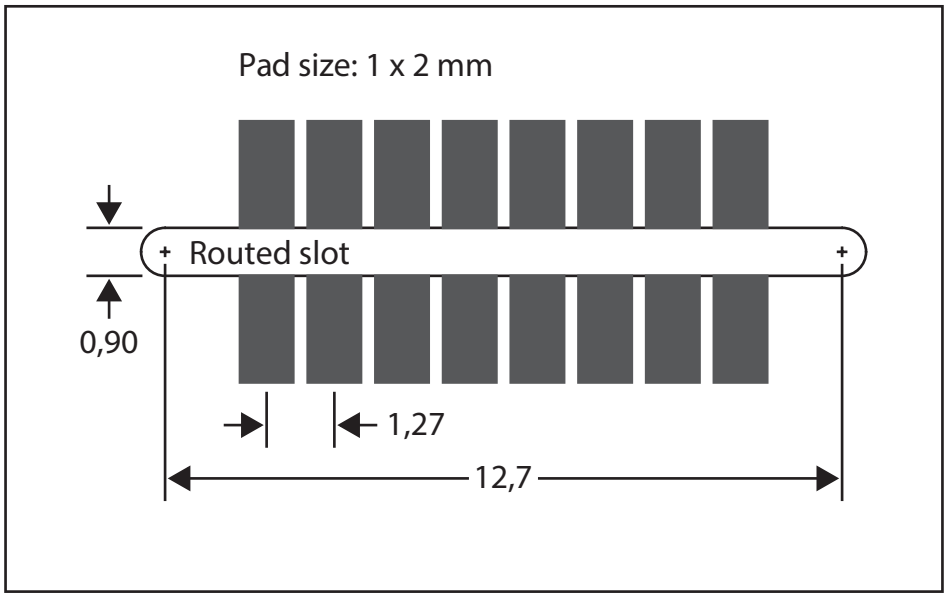
16.4.2 Vertical Mounting

CBM-001 can be mounted in vertical position by using the soldering pads on the narrow end of the module. There are two methods of soldering the module in vertical position. It can be either soldered between pin rows of a 2-row 1,27 mm pin header (2 x 8P) or it can be soldered in a 0,9 mm slot routed on the main board with soldering pads at the edge of the slot. The thickness of the module printed circuit board is 0,85 mm.



Picture 10. Two CBM-001s mounted vertically



Picture 11. Suggested land pattern for vertical mounting in a slot

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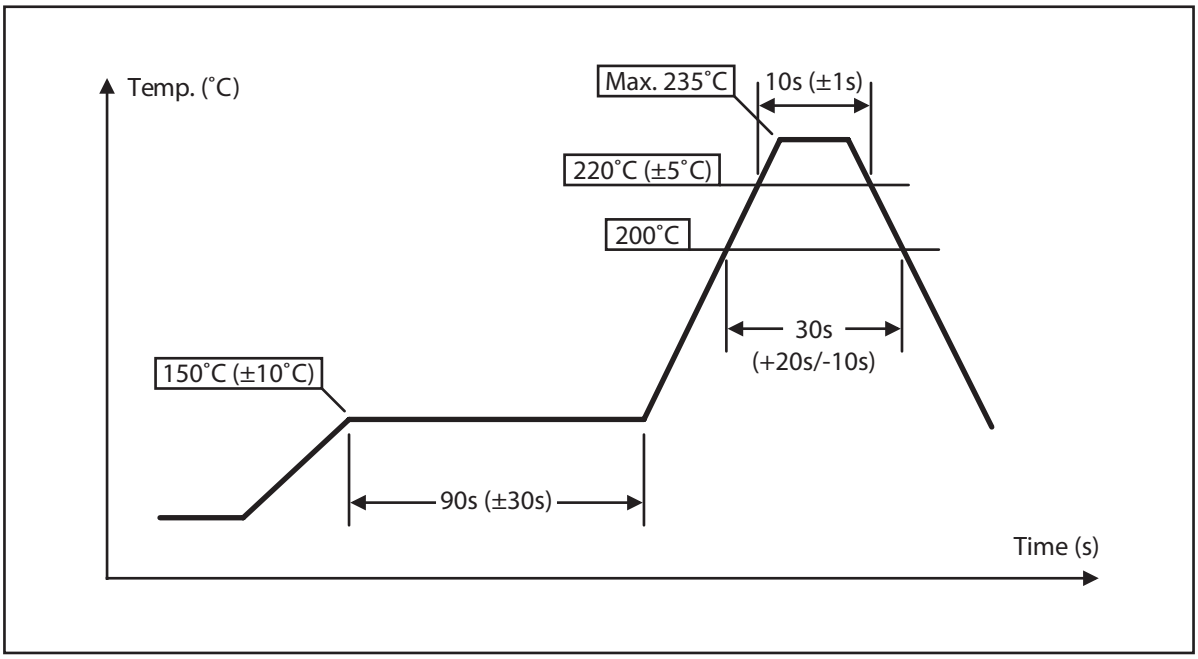
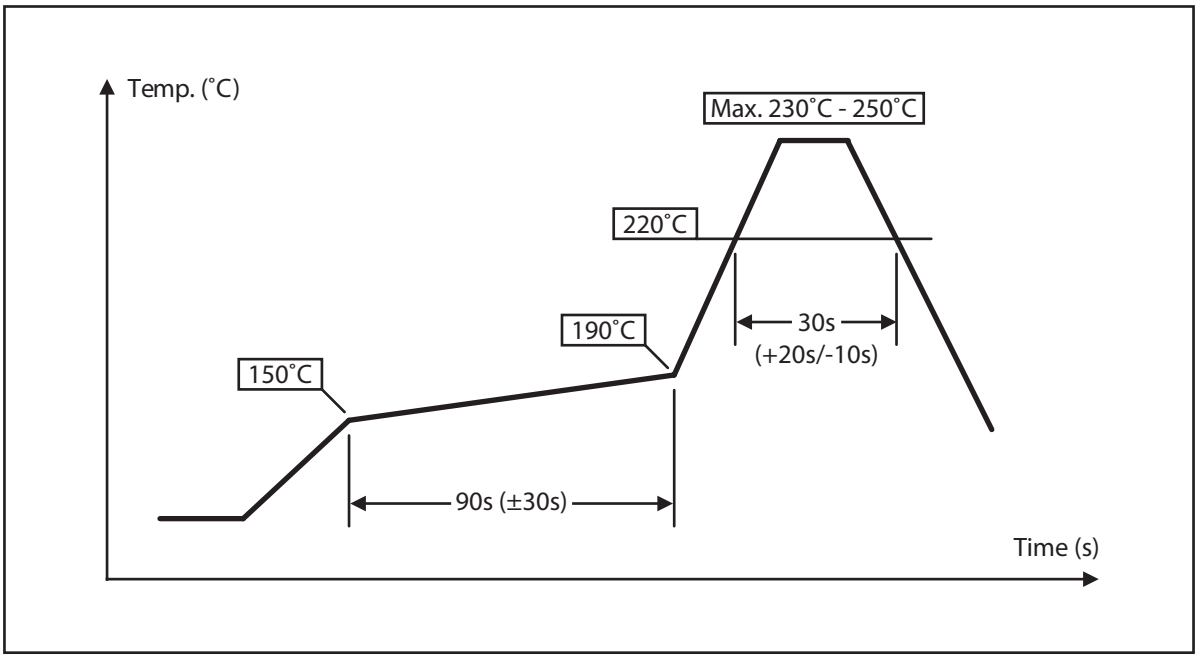
17 Soldering

17.1 Leaded Reflow Soldering



Picture 12. Recommended temperature profile for leaded reflow soldering

17.2 Leadfree Reflow Soldering



Picture 13. Recommended temperature profile for leadfree reflow soldering

Maximum number of reflow cycles: 2
Opposite side reflow is prohibited due to the module's weight. (i.e. you must not place the module on the bottom / underside of your PCB and reflow).

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17.3 Hand Soldering

Hand soldering is possible. When using a soldering iron, follow IPC recommendations (reference document IPC-7711).

17.4 Rework

The module can be unsoldered from the host board. Use of a hot air rework tool should be programmable and the solder joint and module should not exceed the maximum peak reflow temperature of 250°C.

If temperature ramps exceed the reflow temperature profile, module and component damage may occur due to thermal shock. Avoid overheating. Never attempt a rework on the module itself, (e.g. replacing individual components).

17.5 Cleaning

In general, cleaning the populated modules is strongly discouraged. Residuals under the module cannot be easily removed with any cleaning process. Use of "No Clean" soldering paste is strongly recommended, as it does not require cleaning after the soldering process.

18 Compliance Information

Compliance Information		
Radio	USA (not yet approved)	FCC Part 15 Subpart B: 2008 Class B
		FCC Part 15 Subpart B: 2008 Class B
	FCC ID:	TBD
	Europe	ETSI EN 300 328 v1.8.1
	Canada (not yet appr.)	IC RSS-210 low power comm. device
	Certification Number:	TBD
EMC	USA (not yet approved)	FCC CFR47 Part 15 subclass B
	Europe	ETSI EN 301 489-1 v1.9.2
		ETSI EN 301 489-17 v2.2.1
Environmental	RoHS	RoHS compilant

Table 18. Compliance information

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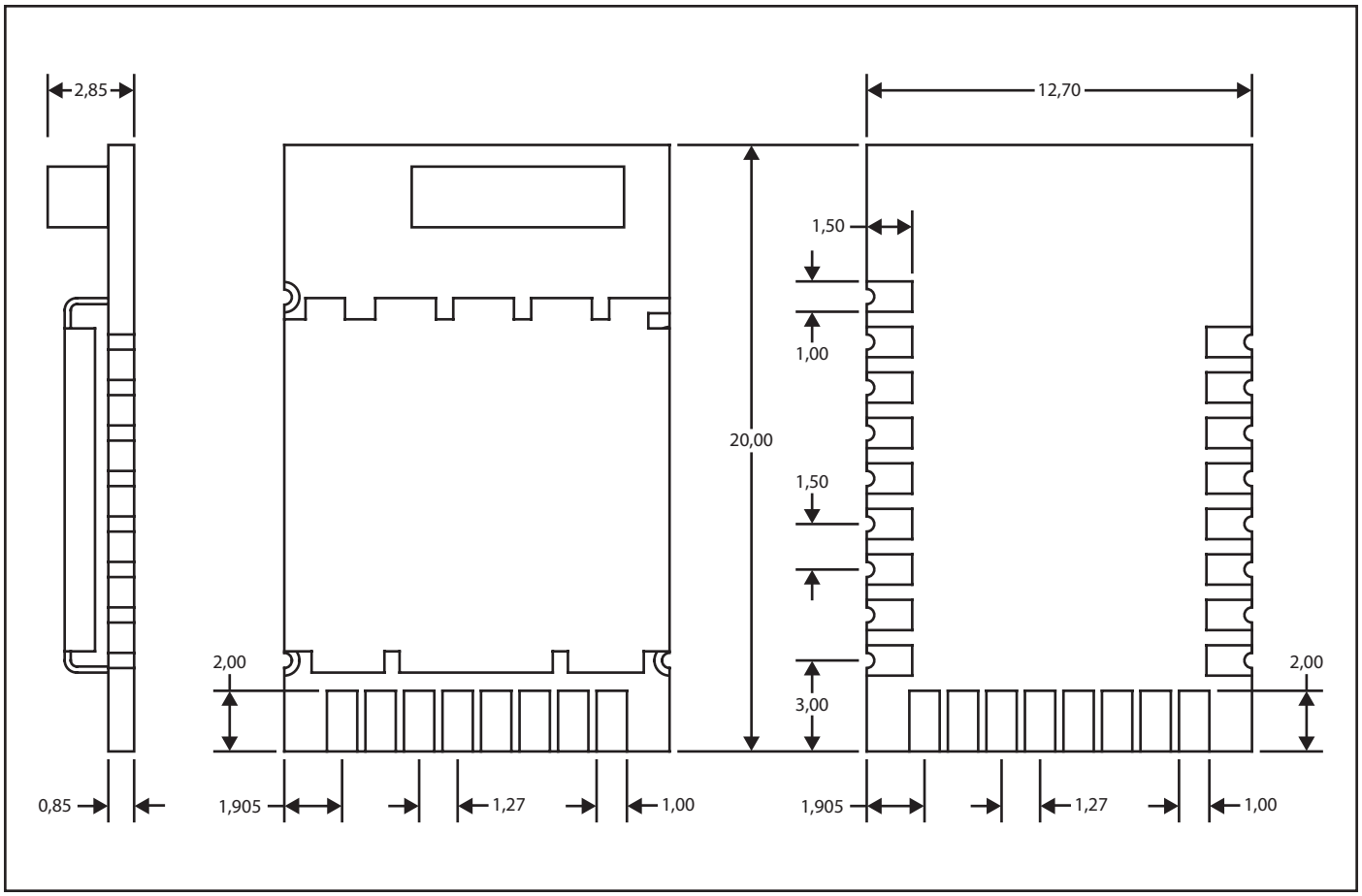
19 Mechanical Specifications



Picture 14. Mechanical dimensions

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